

Application Serial No. 10/572,901  
Reply to office action of February 4, 2008

RECEIVED  
CENTRAL FAX CENTER  
APR 17 2008

PATENT  
Docket: CU-4701

**Amendments To The Claims**

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

**Listing of claims:**

1. **(currently amended)** A voltage controlled digital analog oscillator, comprising:
- an oscillator a frequency of an output signal is determined by a voltage inputted to an analog input end and a digital value inputted to a digital input end; **[[and]]**
- a digital tuner for comparing the voltage inputted to the analog input end with first and second threshold voltages, and changing the digital value inputted to the digital input end according to the result; **and**
- a C-divider adapted to generate a periodic pulse signal (PC) from a reference frequency to drive the digital tuner.**

2. **(currently amended)** The voltage controlled digital analog oscillator according to claim 1, wherein

the oscillator comprises first and second inductors, first and second variable capacitors, first and second NMOS transistors, a current power supply and a **2's multiple number** **an even number plurality** of switched capacitors, wherein:

the first inductor is connected to a higher voltage power supply and a first node;

the second inductor is connected to the higher voltage power supply and a second node;

the first capacitor is connected to the first node and the analog input end;

Application Serial No. 10/572,901  
Reply to office action of February 4, 2008

PATENT  
Docket: CU-4701

the second capacitor is connected to the second node and the analog input end;

a first source and drain is connected to the first node, a gate is connected to the second node, and a second source and drain is connected to a third node, in the first NMOS transistor;

a first source and drain is connected to the second node, a gate is connected to the first node, and a second source and drain is connected to the third node, in the second NMOS transistor;

the current power supply is connected to the third node and a lower voltage power supply;

both ends of half of the switched capacitors are connected between the first node and the lower voltage power supply and switches thereof are connected to the digital input end;

both ends of the remainder of the switched capacitors are connected between the second node and the lower voltage power supply and switches thereof are connected to the digital input end; and

a first output of differential outputs is connected to the first node and a second output is connected to the second node.

3. (original) The voltage controlled digital analog oscillator according to claim 1, wherein the oscillator comprises:

an inductor;

a first variable capacitor having capacitance varied depending on the voltage inputted to the analog input end; and

Application Serial No. 10/572,901  
Reply to office action of February 4, 2008

PATENT  
Docket: CU-4701

a second variable capacitor including a plurality of capacitors, and having capacitance varied by the digital value inputted to the digital input end, wherein the inductor, the first variable capacitor and the second variable capacitor are connected to one another in parallel.

4. (original) The voltage controlled digital analog oscillator according to claim 1, wherein the oscillator comprises:

a variable capacitor having capacitance varied depending on the voltage inputted to the analog input end; and

a variable inductor including a plurality of inductors, and having inductance varied by the digital value inputted to the digital input end, wherein the variable capacitor and the variable inductor are connected to each other in parallel.

5. (original) The voltage controlled digital analog oscillator according to claim 1, wherein the oscillator includes:

a variable inductor including a plurality of inductors, and having inductance varied by the digital value inputted to the digital input end;

a first variable capacitor having capacitance varied depending on the voltage inputted to the analog input end; and

a second variable capacitor including a plurality of capacitors, and having capacitance varied by the digital value inputted to the digital input end, wherein the variable inductor, the first variable capacitor and the second variable capacitor are connected to one another in parallel.

Application Serial No. 10/572,901  
Reply to office action of February 4, 2008

PATENT  
Docket: CU-4701

6. (original) The voltage controlled digital analog oscillator according to claim 1, wherein the digital tuner includes:

a first element for generating an intermittent signal; and

a second element for comparing the voltage inputted to the analog input end with the first and the second threshold voltages, and changing the digital value inputted to the digital input end according to the result, in case where the intermittent signal is generated.

7. (original) The voltage controlled digital analog oscillator according to claim 6, wherein the first element receives a signal having a predetermined frequency, and outputs a signal having a frequency divided by a predetermined integer as the intermittent signal.

8. (original) The voltage controlled digital analog oscillator according to claim 7, wherein the predetermined integer can be changed by a signal given from the exterior.

9. (original) The voltage controlled digital analog oscillator according to claim 6, wherein the second element includes:

a switch for outputting the voltage inputted to the analog input end when the intermittent signal is inputted, and outputting a voltage between the first threshold voltage and the second threshold voltage, otherwise;

a comparator for comparing the output voltage of the switch with the first and the

Application Serial No. 10/572,901  
Reply to office action of February 4, 2008

PATENT  
Docket: CU-4701

second threshold voltages, and outputting the result; and a counter for performing up-counting, down-counting, or no counting according to the output of the comparator.

10. (original) The voltage controlled digital analog oscillator according to claim 9, wherein the value of the counter can be changed by a signal given from the exterior.

11. (original) The voltage controlled digital analog oscillator according to claim 1, wherein a difference between the frequency of the output signal by the first threshold voltage and the frequency of the output signal by the second threshold voltage is larger than a minimum frequency width that can be changed by the change of the digital value, while the digital value is fixed.

12. (currently amended) A frequency synthesizer comprising a phase frequency detector, a current pump, a low pass filter, a digital tuner, an oscillator, a C-divider and a first N-divider divider, wherein:

the phase frequency detector compares frequency and phase of a predetermined input signal with those of an output signal of the first divider, and outputs a signal for controlling the current pump according to the result;

the current pump supplies any one of a positive current and a negative current to the low pass filter depending on the output signal of the phase frequency detector;

the low pass filter receives an output current of the current pump, and outputs a voltage inputted to an analog input end of the oscillator;

the digital tuner intermittently compares the voltage inputted to the analog input

Application Serial No. 10/572,901  
Reply to office action of February 4, 2008

PATENT  
Docket: CU-4701

end of the oscillator with first and second threshold voltages, and changes a digital value inputted to a digital input end of the oscillator according to the result;

the oscillator changes and outputs a frequency of the output signal, depending on the changes of the voltage inputted to the analog input end and the digital value inputted to the digital input end;

**the C-divider adapted to generate a periodic pulse signal (PC) from a reference frequency to drive the digital tuner; and**

the first **N-divider divider** outputs a signal having the frequency of the output signal of the oscillator divided by a first integer **(N)**.

13. (original) The frequency synthesizer according to claim 12, further comprising a second **N-divider divider** for receiving a signal having a predetermined frequency, and inputting a signal having the frequency divided by a second integer **(N+1)**, as the predetermined input signal of the phase frequency detector.

14. (original) The frequency synthesizer according to claim 12, wherein the low pass filter comprises a resistor, and first and second capacitors, wherein:

both ends of the resistor and the first capacitor, which are connected in serial, are connected to a first node and a second node;

the second capacitor is connected to the first node and the second node;

the first node is connected to the input end and the output end; and

the second node is connected to a voltage power supply.

Application Serial No. 10/572,901  
Reply to office action of February 4, 2008

PATENT  
Docket: CU-4701

15. (original) The frequency synthesizer according to claim 12, wherein the digital tuner includes:

a first element for receiving the predetermined input signal of the phase frequency detector, and outputting a signal having a frequency of the signal divided by a third integer, as an intermittent signal; and a second element for comparing the voltage inputted to the analog input end of the oscillator with the first and the second threshold voltages, and changing the digital value inputted to the digital input end of the oscillator according to the result, in case where the intermittent signal is generated.

16. (original) The frequency synthesizer according to claim 12, wherein a difference between the frequency of the output signal of the oscillator by the first threshold voltage and the frequency of the output signal of the oscillator by the second threshold voltage is larger than a minimum frequency width of the output signal of the oscillator that may be changed by the change of the digital value inputted to the digital input end of the oscillator, while the digital value inputted to the digital input end of the oscillator is fixed.

17. (original) A frequency synthesizer comprising a phase frequency detector, a current pump, a low pass filter, a digital tuner, an oscillator and a first divider, wherein:

the phase frequency detector compares frequency and phase of a predetermined input signal with those of an output signal of the first divider, and outputs a signal for controlling the current pump according to the result;

the current pump supplies any one of a positive current and a negative current to the low pass filter depending on the output signal of the phase frequency detector;

Application Serial No. 10/572,901  
Reply to office action of February 4, 2008

PATENT  
Docket: CU-4701

the low pass filter receives an output current of the current pump, and outputs a voltage inputted to an analog input end of the oscillator;

the digital tuner intermittently compares the voltage inputted to the analog input end of the oscillator with first and second threshold voltages, and changes a digital value inputted to a digital input end of the oscillator according to the result;

the oscillator changes and outputs a frequency of the output signal, depending on the changes of the voltage inputted to the analog input end and the digital value inputted to the digital input end; and

the first divider outputs the frequency of the output signal of the oscillator divided by a first integer in a predetermined period, and by a value obtained by adding 1 to the first integer in other periods.

18. (original) The frequency synthesizer according to claim 17, wherein the first divider includes:

a first element for performing an accumulation operation and outputting a signal for determining whether to divide the frequency of the output signal of the oscillator by the first integer, or by the value obtained by adding 1 to the first integer, according to the result; and

a second element for outputting the frequency of the output signal of the oscillator divided by the first integer or the value obtained by adding 1 to the first integer, according to the output signal of the first element.

19. (original) The frequency synthesizer according to claim 17, wherein the digital



Application Serial No. 10/572,901  
Reply to office action of February 4, 2008

PATENT  
Docket: CU-4701

tuner includes:

a first element for receiving the predetermined input signal of the phase frequency detector and outputting a signal having a frequency of the signal divided by a predetermined integer, as an intermittent signal; and

a second element for comparing the voltage inputted to the analog input end of the oscillator with the first and second threshold voltages, and changing the digital value inputted to the digital input end of the oscillator according to the result, in case where the intermittent signal is generated.

20. (original) The frequency synthesizer according to claim 17, wherein a difference between the frequency of the output signal of the oscillator by the first threshold voltage and the frequency of the output signal of the oscillator by the second threshold voltage is larger than a minimum frequency width of the output signal of the oscillator that may be changed by the change of the digital value inputted to the digital input end of the oscillator, while the digital value inputted to the digital input end of the oscillator is fixed.